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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,415	09/20/2000	Kazuyuki Nakagawa	500-0-240	8537

7590 07/24/2002

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/665,415	Nakagama et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Jul 9, 2002 .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-6 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 6
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Amagai (US Pat. 6144102) and Jiang et al (US Pat. 6048755).

Regarding claim 1, the APA (Fig. 4 and 5) discloses a semiconductor device comprising:

- a semiconductor element having a primary surface with an element electrode and a back surface
- a circuit board having a primary surface and a back surface with a board electrode, the circuit board having predetermined opening hole

- the primary surface of the element being bonded to the primary surface of the circuit board by means of an adhesive layer, the adhesive layer being smaller in size than that of the circuit board

- the element electrode of the semiconductor element being connected to the board electrode provided on the back surface of the board via the opening hole, and

- the surrounding regions of the side surfaces of the semiconductor element on the circuit board being sealed with a resin so as to assume a flange structure/shape.

The APA discloses bonding the primary surface of the element with the primary surface of the circuit board by means of an adhesive layer which is of the same size as that of the primary surface of the element but fails to specify using an adhesive layer which is of greater size than that of the primary surface of the element.

Amagai teaches using an adhesive layer (8 in Fig. 7) which is of greater size than that of the primary surface of the element (1 in Fig. 7) to improve rigidity and to reduce stress in a chip size package (Col. 6, line 25-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an adhesive layer which is of greater size than that of the primary surface of the element so that rigidity and stress reduction can be improved using Amagai's device structure in the APA.

Regarding claim 2, the claim elements have been addressed in the rejection as explained above for claim 1.

Regarding claim 3, the APA fails to specify sealing the back surface of the semiconductor element on the circuit board with a resin.

It is conventional in the chip packaging and encapsulation technology art to encapsulate/seal all exposed surfaces of the semiconductor element to provide added protection for the device. Jiang et al teach using a conventional sealing resin/mold (38 in Fig. 1A) surrounding the side surfaces and the back surface of the semiconductor element to provide added protection/sealing for the device (Col. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a resin sealing the side surfaces and the back surface of the semiconductor element on the circuit board so that the surface protection/sealing, rigidity and stress reduction can be improved using Amagai and Jiang et al's structures in the APA.

3. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Amagai (US Pat. 6144102), Jiang et al (US Pat. 6048755) and further in view of Lee et al (US Pat. 6252298) and Miyazaki et al (prior art- IDS reference: Japanese Pat. 09-260535).

Regarding claims 4 and 6, as explained above for claim 1, the APA in view of Amagai teach using the adhesive layer which is of greater size than that of the primary surface of the element in width (X-direction) to improve rigidity but fail to specify the adhesive layer extending radially outwards and completely around the primary surface of the element or extending outside the outer edge of the element without reaching that of the circuit board.

Lee et al teach using a device comprising a composite circuit board and a semiconductor element bonded to the circuit board by an adhesive layer (29 in Fig. 4) where the adhesive layer extends such that the size/area of the adhesive layer/circuit board is slightly greater than that of the semiconductor element as shown (Fig. 4; Col. 4) or could be nearly equal to each other, if desired (Col. 4, line 63). Lee et al do not show the plan/top view of the assembly, however, it would be obvious to one of ordinary skill in the art to realize that size dimensions would be applicable to the dimensions in width and length/longitudinal directions such that the adhesive layer would extending radially outwards and completely around the primary surface of the element.

Furthermore, Amagai teaches using conventional photo/etch processing to form the desired pattern/area of the polyimide/adhesive layer (Col. 6, line 1-25).

Miyazaki et al teach using a BGA device where the adhesive/bonding layer is smaller in size than the primary surface of the substrate/flexible wiring board and does

not reach the outer edge of the board (2 and 3 respectively in Fig. 1 and 2; page 23).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the adhesive layer extending radially outwards and completely around the primary surface of the element or extending outside the outer edge of the element without reaching that of the circuit board so that the surface protection/sealing and rigidity can be improved using Lee et al and Miyazaki et al's adhesive structures in the APA in view of Amagai and Jiang et al.

Regarding claim 5, the claim elements have been addressed in the rejection as explained above for claims 4 and 6.

Response to Arguments

4. Applicant's arguments filed on 07-09-02 have been fully considered but they are not persuasive.

A. Applicant contends that Amagai does not provide any motivation for using a wider adhesive since the contact area between the chip and the adhesive remains the same.

However, as seen from Fig. 7 in Amagai's structure, the adhesive layer (8 in Fig. 7) provides the bonding of the substrate, element, respective wiring/electrode and a

reinforcing part/resin (3, 1 and 20 respectively in Fig. 7). It would be obvious to one of ordinary skill in the art to realize that such bonding layer being greater in size than the element would provide improved adhesion and rigidity for the entire structure. Therefore, Amagai's adhesive structure is applied to the APA.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

07-20-02

Tom Thomas

TOM THOMAS
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